Computer System Architecture COMP201Th Lecture: 10 Sequential Circuits

• Combinational Logic and Sequential Logic are the building blocks of Digital System Design. Combinational Circuits include multiplexers, demultiplexers, encoders, decoders etc. whereas Sequential circuits are Latches, Flip-Flops, Counters, Registers etc.

• Sequential Circuits:

- Sequential logic circuits are those whose output depends not only on the present value of the input but also on previous values of the input signal (history of values) i.e. their output values are computed using both the present and past input values.
- Their output depend on the sequence of input values that have occurred over a period of time. Their dependence on the past input values require the presence of memory elements. The values stored in memory elements define the state of a sequential component.
 - Since memory is finite, therefore the sequence size must always be finite, which means that the sequential logic can contain only a finite number of states → sequential circuits are sometimes called finite- state machines.
- Sequential circuit can be considered as combinational circuit with feedback circuit.



Figure: Sequential Circuit

- The figure above shows a theoretical view of how sequential circuits are made up from combinational logic and some storage elements.
- There are two types of input to the combinational logic:
 - external inputs which come from outside the circuit design and are not controlled by the circuit.
 - Internal inputs which are a function of a previous output states.
- There are two types of sequential circuit:
 - **Synchronous** types uses pulsed or level inputs and a clock input to drive the circuit.
 - **Asynchronous** sequential circuits do not use a clock signal as synchronous circuits do. Instead the circuit is driven by the pulses of the inputs.
- Some terms:
 - **Clock Period:** is the time between successive transitions in the same direction i.e. between two rising or two falling edges.
 - **Clock Frequency** = 1/clock period
 - **Clock width** is the time during which the value of the clock signal is equal to 1.
 - **Active high** if the state changes occur at the clock's rising edge or during the clock width.
 - **Active low** if the state changes occur at the clock's falling edge.



• Flip Flops:

• Flip flops are basic building block of sequential circuits. Flip flops store a single binary digit of a state. It has two stable states i.e. it is bistable which means it is stable in each state means when put in a specific state, it will stay in that state until something causes it to change to the other state. The output stays low or high, to change it the circuit must be derived by an input called trigger.

• Triggering:

- The change in the output of a flip flop can be done by bringing a small change in the input signal. This small change can be done with the help of a clock pulse. This clock pulse is known as a trigger pulse.
- There are two types of triggering:
 - Level Triggering and
 - Edge Triggering
- Level Triggering:
 - The triggering process in which the change in the output state is according to the active level of inputs is called level triggering. Its of two types:
 - High Level Triggering
 - Low Level Triggering
 - High Level Triggering:
 - In high level triggering, the output of the flip-flop changes only when its enable input is at a high state i.e. logic high or logic 1.



- Low Level Triggering:
 - In low level triggering, the output of the flip-flop changes only when its enable input is at a low state i.e. logic low or logic 0.

Triggering on low clock level



Edge Triggering:

- In Edge Triggering, the output changes only when the inputs are present at either of the transitions of the clock pulse i.e. either from low to high (0 to 1) or from high to low (1 to 0). Edge triggering is of two types, they are:
 - Positive Edge Triggering
 - Negative Edge Triggering

• Positive Edge Triggering

- In positive edge triggering, the output changes only when the input is at the positive edge of the clock pulse input i.e. a transition from low to high (0 to 1).
- Positive Edge Triggering method is used when a flipflop is required to respond at low to high level transition state.

Triggers on this edge of clock pulse



• Negative Edge Triggering:

- In negative edge triggering, the output changes only when the input is at the negative edge of the clock pulse input i.e. a transition from high to low (1 to 0).
- Negative Edge Triggering method is used when a flipflop is required to respond at high to low level transition state.

Triggers on this edge of clock pulse

