Computer System Architecture
COMP201Th
Lecture: 12
SR & JK Flip Flop

- **Characteristic Table:**
  - The characteristic table of flip-flops specifies the next state when the inputs and the present states are known.
  - Used in analysis

S R Flip-Flop			
S	***R***	***Q(t + 1)***	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	X	Invalid

Characteristic table for SR flip flop

- **Characteristic Equation:**
  - Defines the next state of the flip-flop as a Boolean equation of the flip-flop inputs and the current state. Characteristic equation for SR flip flop is:

$$Q(t+1) = S+R`Q(t)$$

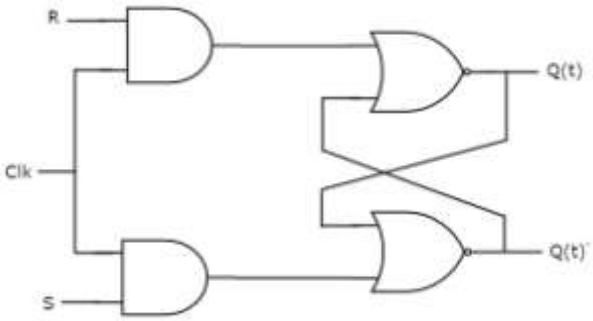
- **Excitation Table:**
  - Defines the flip-flop input variable values as function of the current state and the next state.
  - Used in design.
  - ***Example:*** Consider the SR flip-flop:

Q(t)	Q(t+1)	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

Excitation Table for S-R flip flop.

- Excitation table consists of two columns Q(t) and Q(t+1) and a column for each input to show how the required transition is achieved. There are four possible transitions from present state Q(t) to next state Q(t+1). The required input condition for each of these transitions are derived from the information available in the characteristic tables. The symbol **x** in the table represents a don't care condition i.e. it does not matter whether the input to the flip flop is 0 or 1.
- The reason for the don't care conditions in the excitation tables is that there are two ways of achieving the required transition. E.g. in SR flip flop; a transition from present state of 0 to a next state of 0 can be achieved by having inputs S and R equal to 0 (to obtain no change) or by letting S =0 and R=1 to clear the flip flop (clear to 0/ Reset). In both cases, S must be 0 but R can be either 0 or 1. Since, the required transition will occur in either case, we mark the R input with a don't care **X** and let the designer choose either 0 or 1 for the R input, whichever is more convenient.

- **SR Flip Flop:**
  - SR flip flop is also known as gated or clocked SR latch.
  - In this, the output is changed (i.e. the stored data is changed) ***only when you give an active clock signal*** otherwise even if the S or R is active the data will not change.



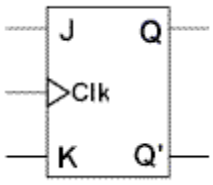
S R Flip-Flop			
S	*R*	*Q*(*t* + 1)	
0	0	*Q*(*t*)	No change
0	1	0	Reset
1	0	1	Set
1	1	*X*	Invalid

Characteristic Table For SR flip flop

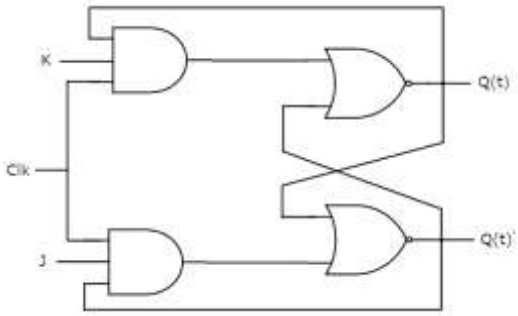
Q(t)	Q(t+1)	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

Excitation table for SR Flip flop

- **JK Flip Flop:**
  - JK flip flop is an improvement on the SR flip flop where S=R=1 is not a problem.
  - JK flip flop is basically an SR flip flop with feedback which enables only one of its two input terminals either SET or RESET to be active at any one time thereby eliminating the invalid condition of SR flip flop.
  - When both J & K inputs are at logic level '1' at the same time and the clock input is pulsed high the circuit will toggle from its SET state to a RESET state or vice-versa.



Graphic Symbol for JK Flip flop



Logic Diagram for JK flip flop

Characteristic Equation for JK flip flop is:

Q(t+1) = JQ`+K`Q

Characteristic table for JK flip flop is:

J	**K**	**Q(t+1)**
0	0	Q(t) No change
0	1	0 Clear to 0
1	0	1 Set to 1
1	1	Q`(t) Complement

Excitation table for JK flip flop is:

Q(t)	**Q(t+1)**	**J**	**K**
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0