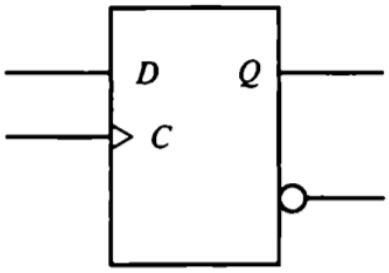
**Computer System Architecture**
**COMP201Th**
**Lecture: 13**
**D flip flop and T flip flop**

- **D Flip-Flop:**
  - The D (data) flip-flop is a slight modification of the SR flip-flop.
  - An SR flip-flop is converted to a D flip-flop by inserting an inverter between S and R and assigning the symbol D to the single input.
  - If D=1, the output of the flip-flop goes to the 1 state, but if D=0, the output of the flip flop goes to the 0 state.
  - The D input is sampled during the occurrence of a clock transition from 0 to 1. This means that the Q output of the flip-flop receives its value from the D input every time that the clock signal goes through a transition from 0 to 1.




(a) Graphic symbol

| D | Q (t + 1) | |
|---|---|---|
| 0 | 0 | Clear to 0 |
| 1 | 1 | Set to 1 |

(b) Characteristic table

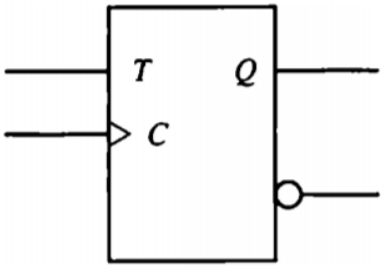
  - From the characteristic table, we can say that the next state Q(t+1) is determined from the D input. The relationship can be expressed by a characteristic equation:

$$Q(t+1) = D$$

  - Although, a D flip-flop has the advantage of having only one input (excluding C), it has the disadvantage that its characteristic table does not have a no change condition Q(t+1) = Q(t). The "no change" condition can be accomplished either by disabling the clock signal or by feeding the output back into the input, so that clock pulses keep the state of the flip flop unchanged.

- **T Flip-Flop:**
  - T(toggle) flip-flop is obtained from a JK type when inputs J and K are connected to provide a single input designated by T.
  - The T flip-flop therefore has only two conditions:
    - When T = 0 (J=K=0) a clock transition does not change the state of the flip-flop.
    - When T = 1 (J=K=1) a clock transition complements the state of the flip flop.
  - These conditions can be expressed by a characteristic equation:

$$Q(t+1) = Q(t) \oplus T$$

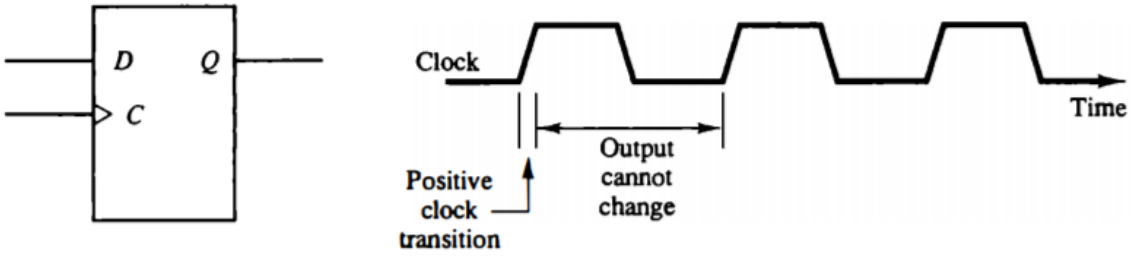



(a) Graphic symbol

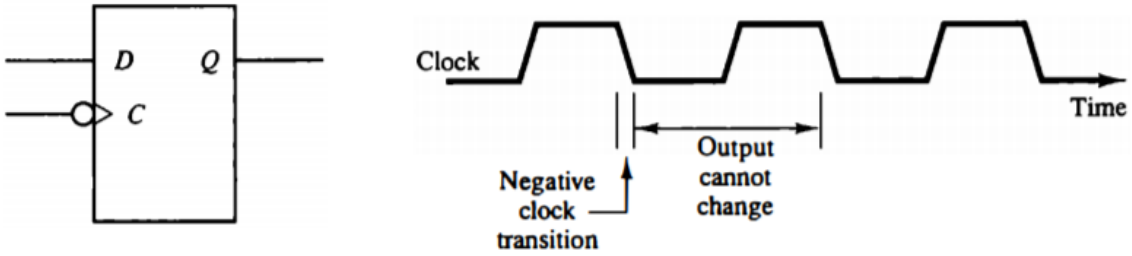
| $T$ | $Q(t+1)$ | |
|---|---|---|
| 0 | $Q(t)$ | No change |
| 1 | $Q'(t)$ | Complement |

(b) Characteristic table

- **Edge-Triggered Flip-Flops:**
  - The most common type of flip-flop used to synchronize the state change during a clock pulse transition is the edge-triggered flip –flop.
  - In this type of flip-flop, output transitions occur at a specific level of the clock pulse.
  - When the pulse input level exceeds this threshold level, the inputs are locked out so that the flip-flop is unresponsive to further changes in inputs until the clock pulse returns to 0 and another pulse occurs.
  - Some edge-triggered flip-flops cause a transition on the rising edge of the clock pulse (positive-edge transition) and others cause a transition on the falling edge (negative-edge transition).




(a) Positive-edge-triggered *D* flip-flop.

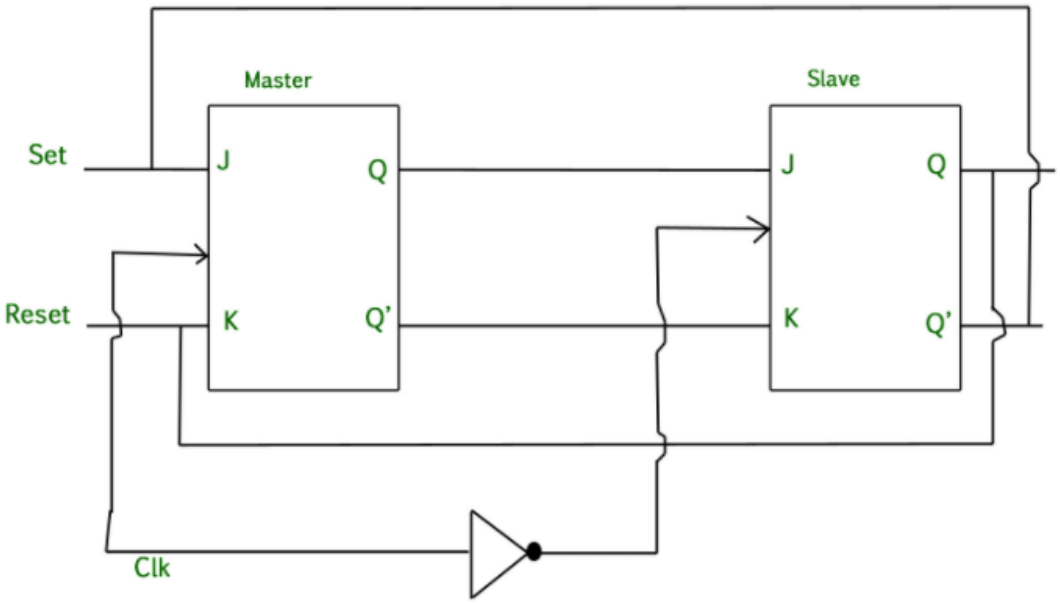



(b) Negative-edge-triggered *D* flip-flop.

- Fig (a) above shows the clock pulse signal in a positive-edge triggered D flip flop. The value in the D input is transferred to the Q output when the clock makes a positive transition. The output cannot change when the clock is in the 1 level, in the 0 level or in a transition from the 1 level to the 0 level.
- Fig (b) shows the corresponding graphic symbol and timing diagram for negative-edge-triggered D flip flop. The graphic symbol includes a negation small circle in front of the dynamic indicator at the C input. This denotes a negative-edge triggered behavior. In this case, the flip-flop responds to a transition from the 1 level to the 0 level of the clock signal.

- **Master Slave JK Flip-Flop:**
  - **Race Around Condition in JK Flip-Flop:**
    - For JK flip flop, if J=K=1 and if CLK=1, for a long period of time, then Q output will toggle as long as CLK is high, which makes the output of the flip flop unstable or uncertain.
      - This problem is called race around condition in JK flip flop.
      - It can be avoided by ensuring that the clock input is at logic 1 only for a very short time. This introduced the concept of Master JK flip flop.

- The Master Slave Flip Flop is basically a combination of two JK flip flops connected together in a series configuration. Out of these, one acts as the master and the other as a slave.
- The output from the master flip flop is connected to the two inputs of the slave flip flop whose output is fed back to inputs of the master flip flop.
- In addition to these two flip-flops, the circuit also includes an inverter. The inverter is connected to clock pulse in such a way that the inverted clock pulse is given to the slave flip flop i.e. if clock pulse (CP) = 0 for a master flip flop, then CP=1 for a slave flip flop and vice versa.




Master-slave JK Flip-Flop