Computer System Architecture
COMP201Th
Lecture: 14
Registers

A register is a group of flip-flops with each flip-flop capable of storing one bit of information. An n-bit register has a group of n flip-flops and is capable of storing any binary information of n bits. In addition to flip-flops, registers also consists of gates that effect their transition. The flip-flops hold the binary information and the gates control when and how new information is transferred into the register.

The simplest register is one that consist out of flip-flops with no external gates.

e.g. Fig below shows a simple 4-bit register constructed with four D flip-flops.

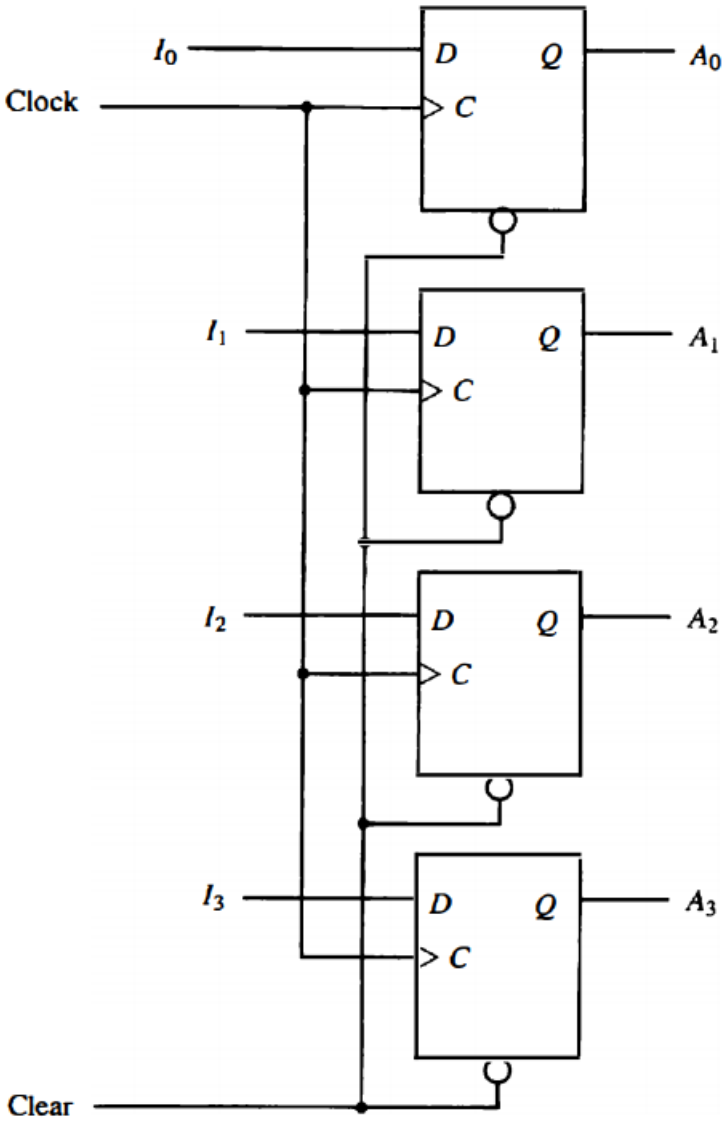
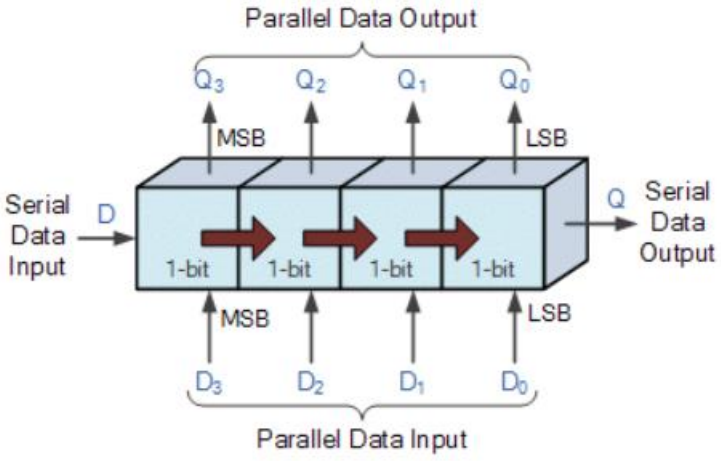


Fig: 4-bit register

- The common clock input triggers all flip-flops on the rising edge of each pulse and the binary data available at the four inputs are transferred into the 4-bit register.
- The four outputs can be sampled at any time to obtain the binary information stored in the register.
- The Clear input goes to a special terminal in each flip-flop.
    - When the input goes to 0, all flip-flops are reset asynchronously.
    - The clear input is useful for clearing the register to all 0's prior to its clock operation.
    - The clear input must be maintained at logic 1 during normal clocked operation.
- **Register Load:**
    - The transfer of new information into a register is referred to as loading the register.
    - If all the bits of the register are loaded simultaneously with a common clock pulse transition, we say that the loading is done in parallel.

Shift Registers:

- A register capable of shifting its binary information in one or both directions is called a shift register.
- Bits enter the shift register at one end and emerge from the other end. The two ends are called left and right. When a bit is input on the left, all the bits in the register move one place to the right and the rightmost bit disappears. When a bit is input to the right, all the bits move one place to the left and the leftmost bit disappears.



- The logical configuration of a shift register consists of a chain of flip-flops in cascade, with the output of one flip-flop connected to input of the next flip-flop.
    - All flip-flops receive common clock pulse that initiate the shift from one stage to the next.

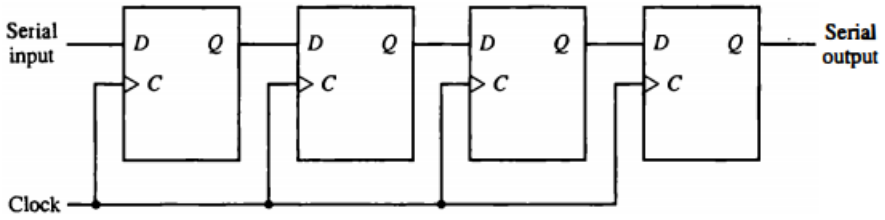


Fig: 4-bit shift register

- As shown in fig above the output of a given flip-flop is connected to the D input of the flip-flop at its right. The clock is common to all flip-flops. The serial input determines what goes in to the leftmost position during the shift. The serial output is taken from the output of the rightmost flip-flop.
- Shift Registers are used for data storage or for the movement of data and are therefore commonly used inside calculators or computers to store data such as two binary numbers before they are added together or to convert data from either a serial to parallel or parallel to serial format. i.e. shift registers are commonly used in converters that translate parallel data to serial data or vice versa.

- **The most general shift register has following capabilities:**
    - An input for clock pulses to synchronize all operations.
    - A shift-right operation and a serial input line associated with the shift-right.
    - A shift-left operation and a serial input line associated with the shift-left.
    - A parallel load operation and n input lines associated with the parallel transfer.
    - n parallel output lines.
    - A control state that leaves the information in the register unchanged even though clock pulses are applied continuously.

Bidirectional Shift Register with Parallel Load:

- A register capable of shifting in one direction only is called a unidirectional shift register. A register that can shift in both directions is called a bidirectional shift register.
- A 4-bit bidirectional shift register with parallel load is shown in fig below:

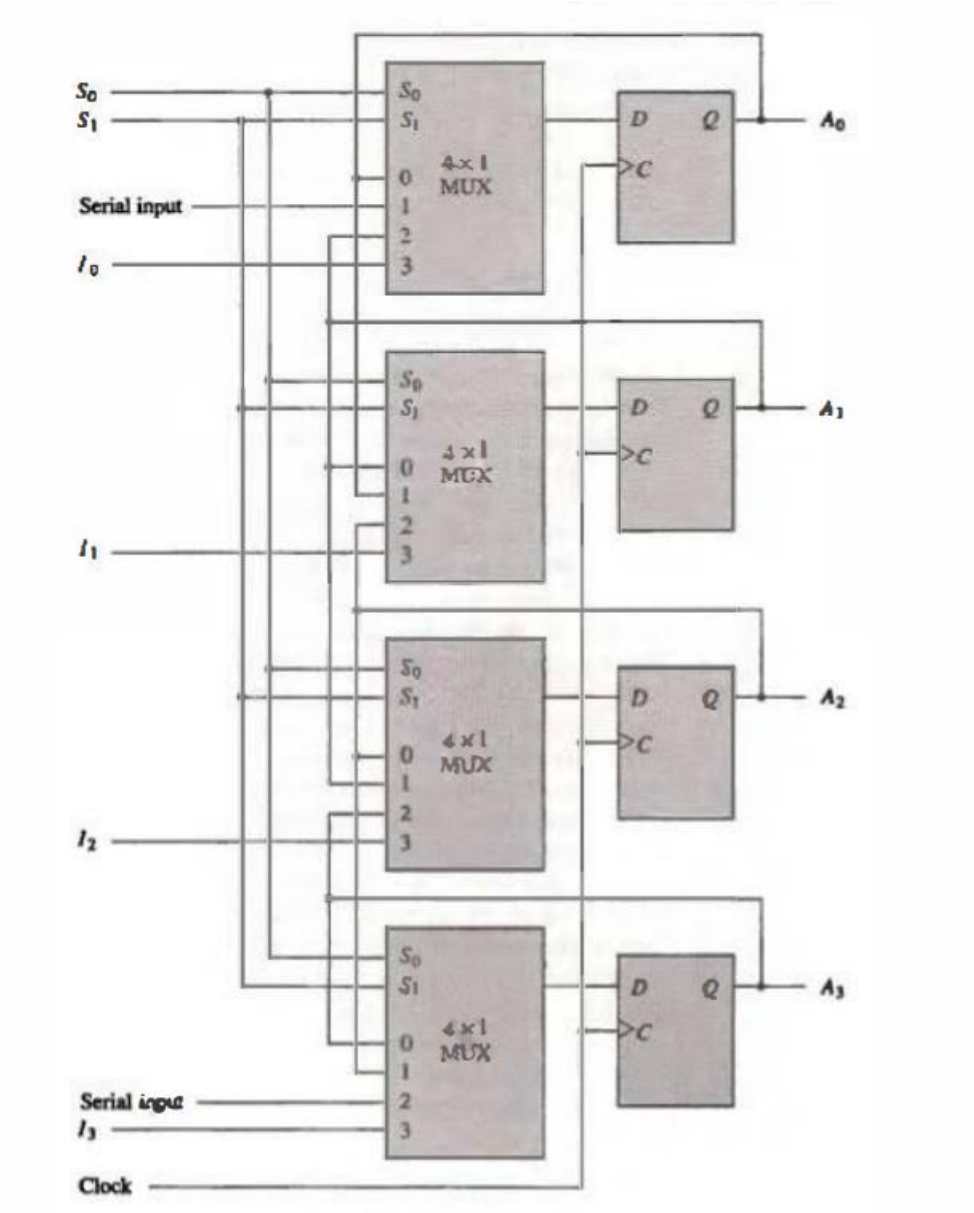


Fig. : Bidirectional Shift Register with Parallel Load

In the above diagram (the way it's drawn),shift-right operation shifts the contents of the register in the down direction while the shift left operation causes the contents of the register to shift in the upward direction.

In the above fig:

- Each stage consists of a D flip flop and a 4*1 multiplexer.
- The two selection inputs S1 and S0 select one of the multiplexer data inputs for the D flip flop.
- The selection lines control the mode of operation of the register according to the function table as below:

Mode control		
S_1	S_0	Register operation
0	0	No change
0	1	Shift right (down)
1	0	Shift left (up)
1	1	Parallel load

- When the mode control is S1S0=00
    - data input 0 of each multiplexer is selected. This condition forms a path from the output of each flip flop into the input of the same flip-flop.
    - The next clock transition transfers into each flip flop the binary value it held previously and no change of state occurs.

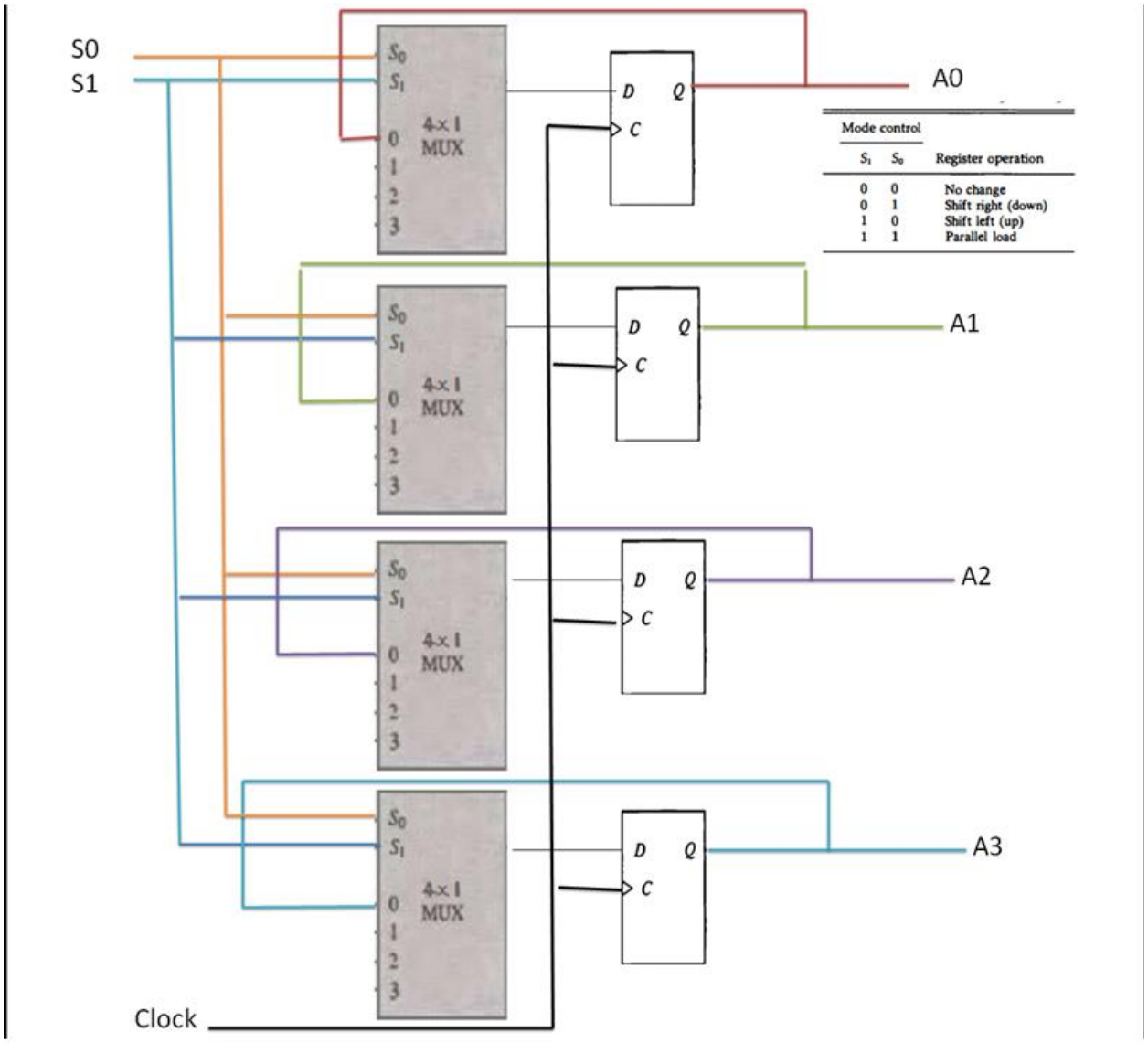


Fig: When S1S0=00

- When S1S0=01:
    - the terminal marked 1 in each multiplexer has a path to the D input of the corresponding flip flop. This causes a shift-right operation, with the serial input data transferred into flip-flop A0 and the content of each flip flop Ai-1 transferred into flip flop Ai for i=1,2,3.

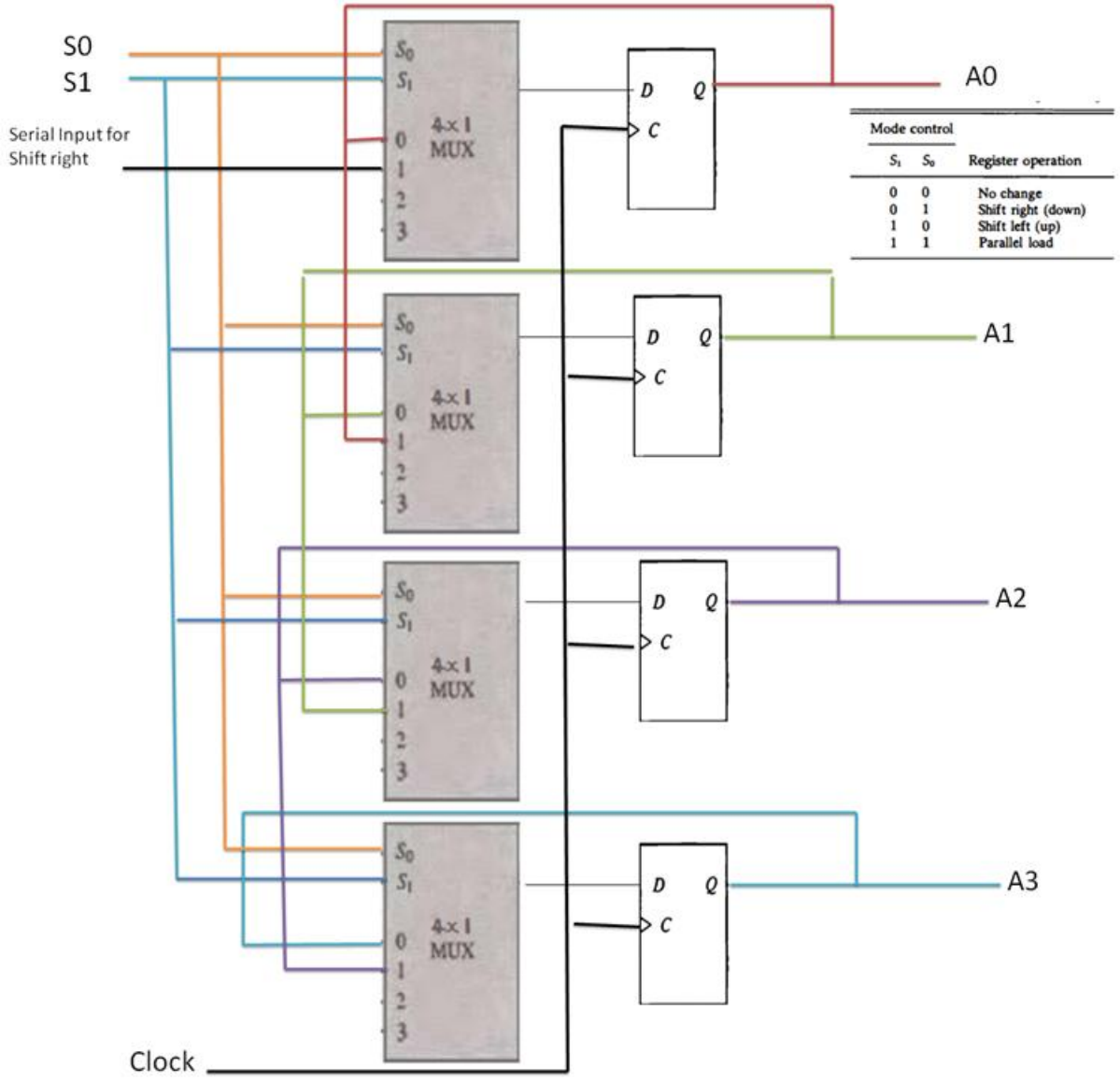


Fig: S1S0=01

- When S1S0=10:
    - A shift left operation results with the other serial input data going into flip-flop A3 and the content of flip-flop Ai+1 transferred into flip flop Ai for i=0,1,2.

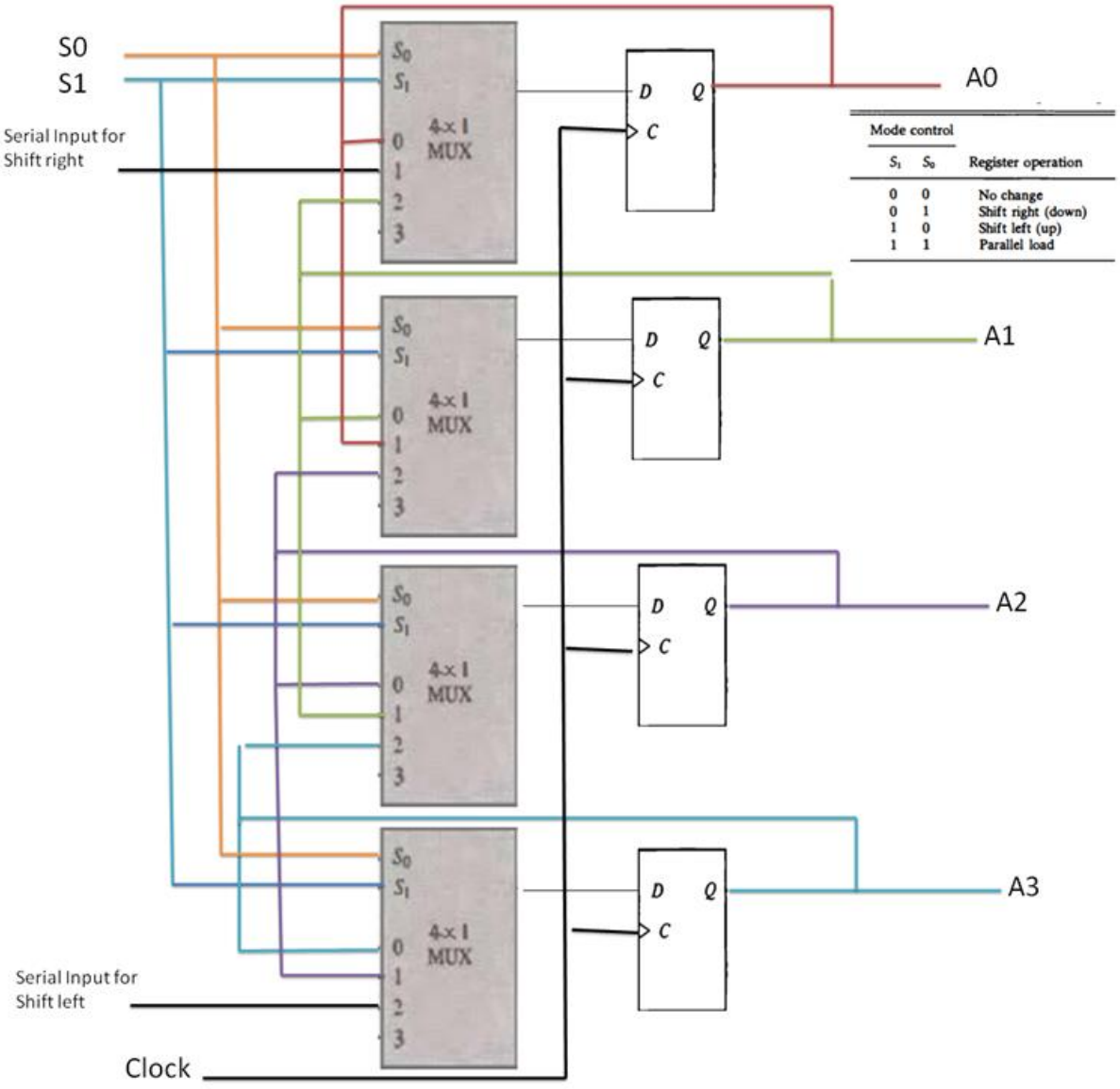


Fig: S1S0=10

- When S1S0=11
    - the binary information from each input I0 through I3 is transferred into the corresponding flip-flop, resulting in a parallel load operation.