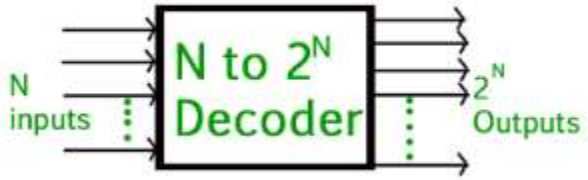
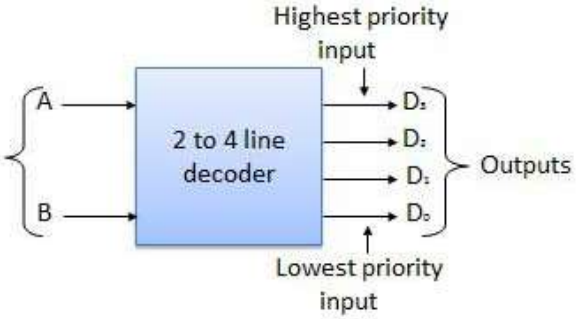
Computer System Architecture
COMP201Th
Lecture: 9
Decoders

Discrete quantities of information are represented in digital computers with binary codes. A binary code of n bits is capable of representing upto 2^n distinct elements of the coded information.

- **Decoders:**
  - A decoder is a combinational circuit that converts binary information from the n coded inputs to a maximum of 2^n unique outputs.
  - A decoder has n inputs and m outputs and is also referred to as n × m decoder.
  - Decoding is essential in applications like memory address decoding and 7 segment display.



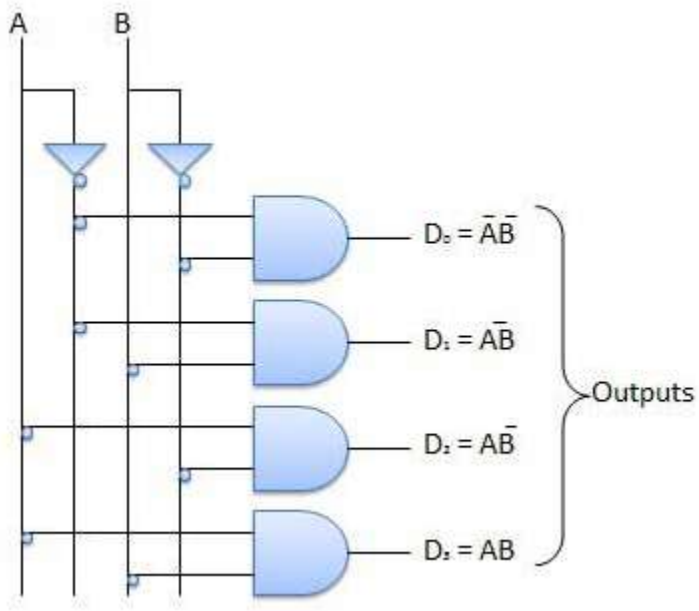
- **2 to 4 Decoder:**
  - 2 to 4 decoder has two inputs and 4 outputs.



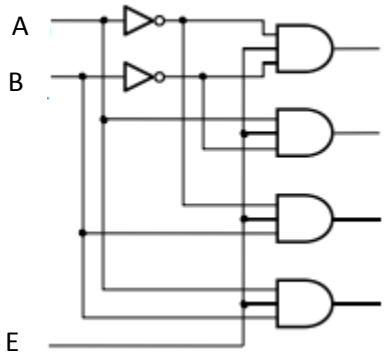
  - Decoder have two inputs namely A, B and four outputs denoted by D0,D1,D2,D3. The truth table for 2 to 4 decoder is:

Inputs		Output			
A	B	D0	D1	D2	D3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

- Logic circuit for 2 to 4 decoder is as below:

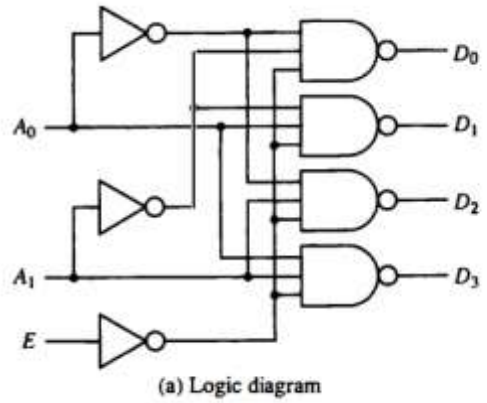


- Commercial decoders include one or more enable inputs to control the operation of the circuit. The decoder is enabled when E is equal to 1 and disabled when E is equal to 0.



- ***Enable inputs are a convenient feature for interconnecting two or more circuits for the purpose of expanding the digital component into a similar function but with more inputs and outputs.***

- **NAND Gate Decoder:**
  - Its more economical to use NAND instead of AND gates as they are easy to fabricate.



(a) Logic diagram

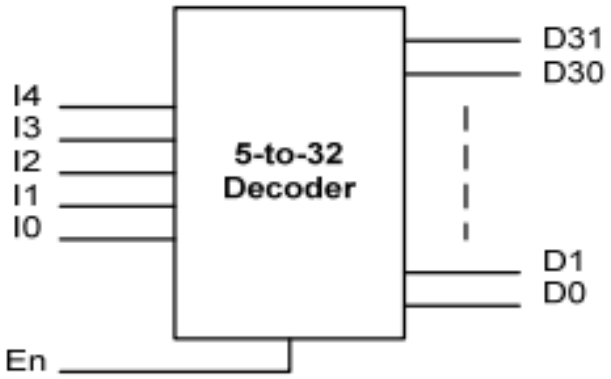
E	A_1	A_0	D_0	D_1	D_2	D_3
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0
1	×	×	1	1	1	1

(b) Truth table

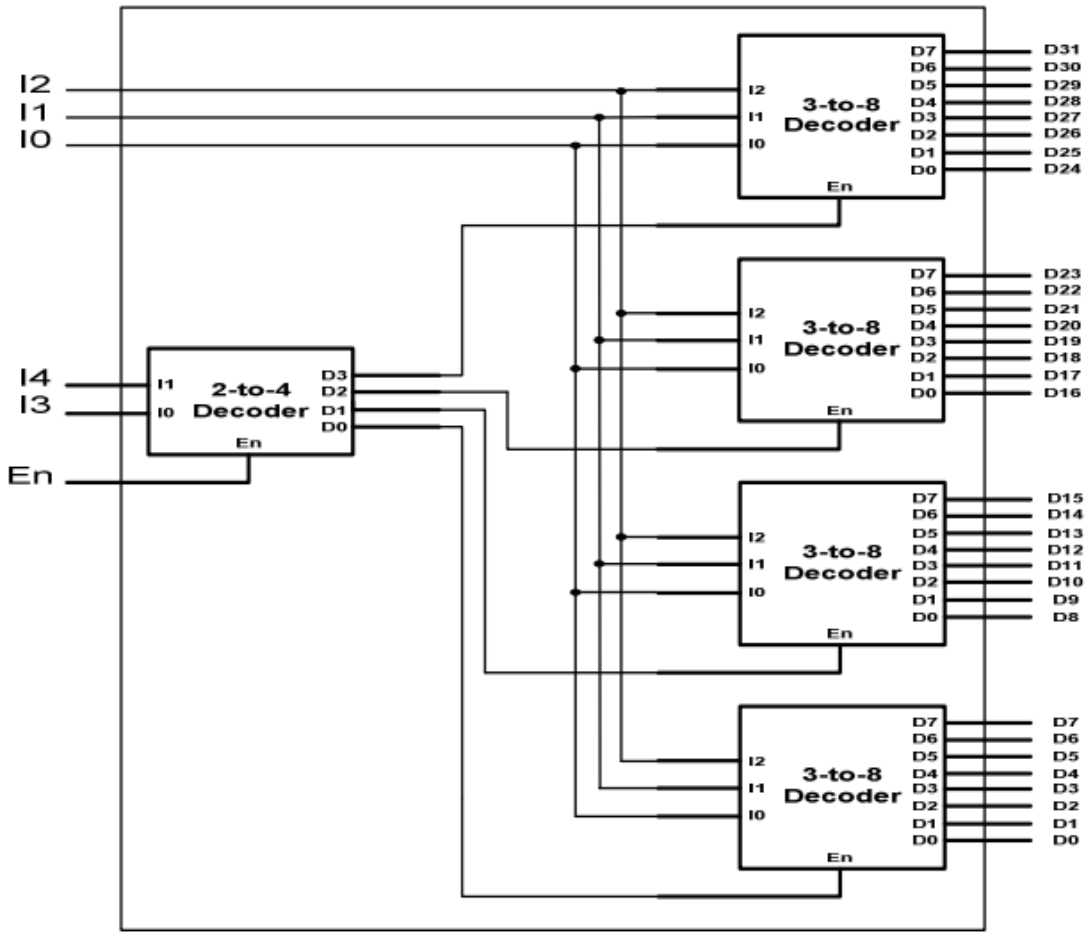
Fig. 2 to 4 Decoder using NAND gates.

  - **In general a decoder may operate with complemented or uncomplemented outputs.**

- **Decoder Expansion:**
  - It is possible to combine two or more decoders with enable inputs to form a larger decoder.
  - e.g. Construct a 5 to 32 line decoder using 3 to 8 line decoder with Enable and 2 to 4 line decoder.



Here output is 32 so we can say that we need four 3to 8 decoder and to select (i.e. to Enable them) we need one 2 to 4 decoder.



- ***Any combinational circuit with n inputs and m outputs can be implemented with an n to 2^n line decoder and m OR gates.***