Computer System Architecture
COMP201Th
Lecture: 15
Counters

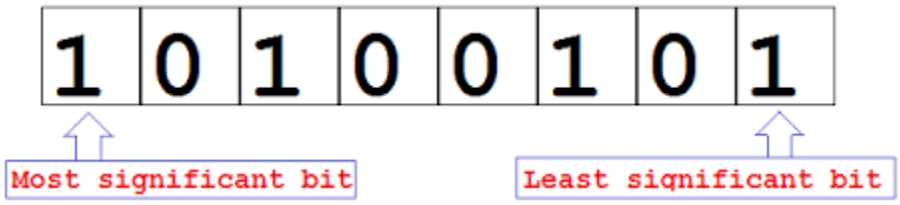
A register that goes through a predetermined sequence of states upon the application of input pulses is called a counter.

- The input pulse may be clock pulses or may originate from an external source. They may occur at uniform intervals of time or at random.

A counter simply counts i.e. if it is at 1 then next time it will say 2, then 3 and so on.

There may be counter which counts from 0 to 10 or there may be counter which will count from 2 to 6, so it all depends on the design of the counter.

Always remember for binary numbers LSB and MSB are:



Binary Counter:

- A counter that follows the binary number sequence is called a binary counter.
- An n-bit binary counter is a register of n flip-flops and associated gates that follows a sequence of states according to the binary count of n bits from 0 to 2^n-1.
- The key to building a counter is bit pattern of binary numbers.
    - The least-significant bit toggles every time the number is incremented.
    - Every other bit is complemented from on count to the next if and only if all its lower-order bits are equal to 1.

Binary	Decimal
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9
1010	10
1011	11
1100	12
1101	13
1110	14
1111	15

A counter circuit will usually employ flip-flop with complementing capabilities. Both T and JK flips have this property.

- JK flip flop is complemented if both its J and K inputs are 1 and the clock goes through a positive transition.
- The output of the flip flop does not change if J=K=0.

4- bit Synchronous Binary Counter:

The circuit of 4 bit synchronous binary counter is shown below:

The first stage (of FF0) i.e. Q_0 is complemented when the counter is enabled and the clock goes through a positive transition. Each of the other three flip-flops are complemented when all previous least significant flip-flops are equal to 1. The AND gates generate the required logic for the J and K inputs.

Note: For detailed working, do watch the lecture video. I will explain in the video, you may note down the important points from there in your notes.

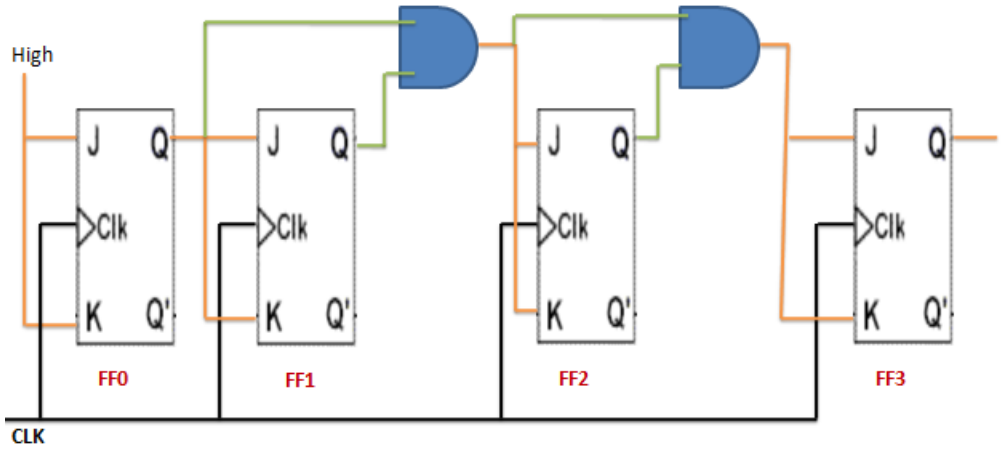


Fig: 4 bit Synchronous binary counter