Unit: 4
Input-Output Organization
Lecture-4
Priority Interrupt

In a typical application, a number of I/O devices are attached to the computer, with each device being able to originate an interrupt request. The first task of the interrupt system is to identify the source of the interrupt. There is also the possibility that several sources will request service simultaneously. In this case the system must also decide which device to service first.

Priority Interrupt:

- A priority interrupt is a system that establishes a priority over the various sources to determine which condition is to be services first when two or more requests arise simultaneously.
- Higher priority interrupt levels are assigned to requests which, if delayed or interrupted could have serious consequences.
- Devices with high speed transfers such as magnetic disks are given high priority and slow devices such as keyboards receive low priority.

When two devices interrupt the computer at the same time, the computer services the devices with the higher priority first.

Establishing the priority of simultaneous interrupts can be done by software or hardware:

- **Software:** Polling
- **Hardware:** Daisy chain, Parallel Priority

Polling: A polling procedure is used to identify the highest-priority source by software means.

- In this method, there is one common branch address for all interrupts.
- The program that takes care of interrupts begins at the branch address and polls the interrupt sources in sequence.
- The order in which they are tested determines the priority of each interrupt.

The disadvantage of the software method is that if there are many interrupts, the time required to poll them can exceed the time available to service the I/O device.

➔ a hardware priority interrupt unit can be used to speed up the operation.

A hardware priority-interrupt unit functions as an overall manager in an interrupt system environment. It accepts interrupt requests from many sources, determines which of the incoming requests has the highest priority, and issues an interrupt request to the computer based on the determination.

Daisy-Chaining Priority: The daisy-chaining method of establishing priority consists of a serial connection of all devices that request an interrupt.

- The device with the highest priority is placed in the first position, followed by the lower-priority devices up to the device with the lowest priority, which is placed last in the chain.

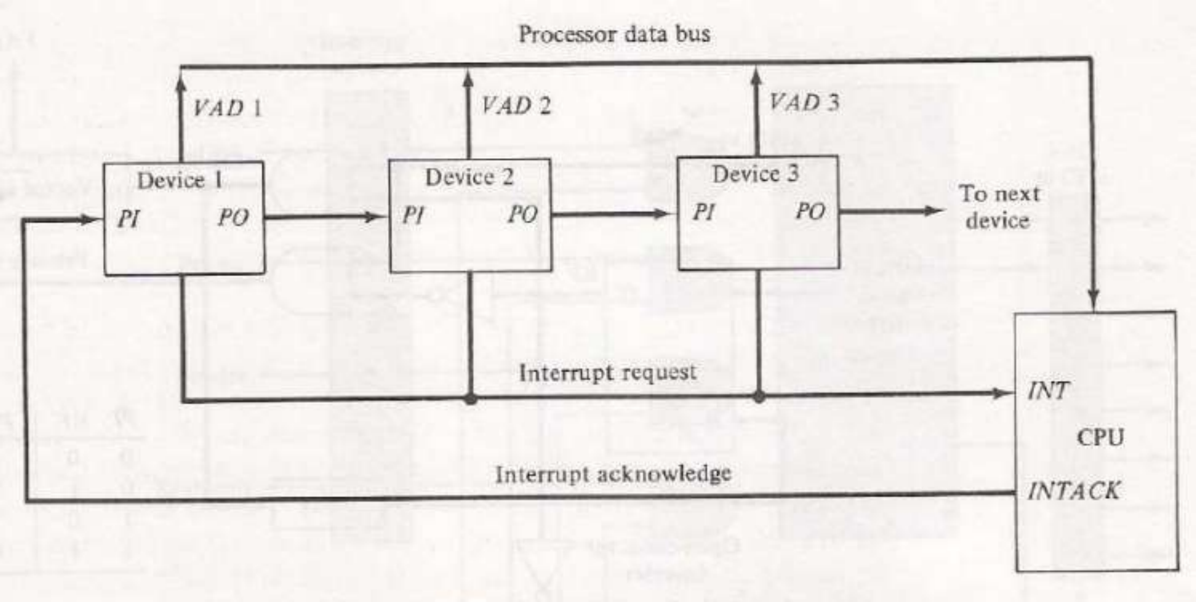

Figure Daisy-chain priority interrupt.

- The interrupt request line is common to all devices and forms a wired logic connection.
- If any device has an interrupt signal in the low-level state, the interrupt line goes to the low-level state and enables the interrupt input in the CPU.
- When no interrupts are pending, the interrupt line stays in the high-level state and no interrupts are recognized by the CPU.
    - → this is equivalent to the negative logic OR operation.
- The CPU responds to an interrupt request by enabling the interrupt acknowledge line. This signal is received by device 1 at its PI (Priority In) input.
- The acknowledge signal passes on to the next device through the PO (Priority Out) output only if device 1 is not requesting an interrupt.
- If device 1 has a pending interrupt, it blocks the acknowledge signal from the next device by placing a 0 in the PO output.

Parallel Priority Interrupt:

The parallel priority interrupt method uses a register whose bits are set separately by the interrupt signal from each device.

- Priority is established according to the position of the bits in the register.
- Mask register is used to provide facility for the higher priority devices to interrupt when lower priority device is being serviced or disable all lower priority devices when higher is being services.

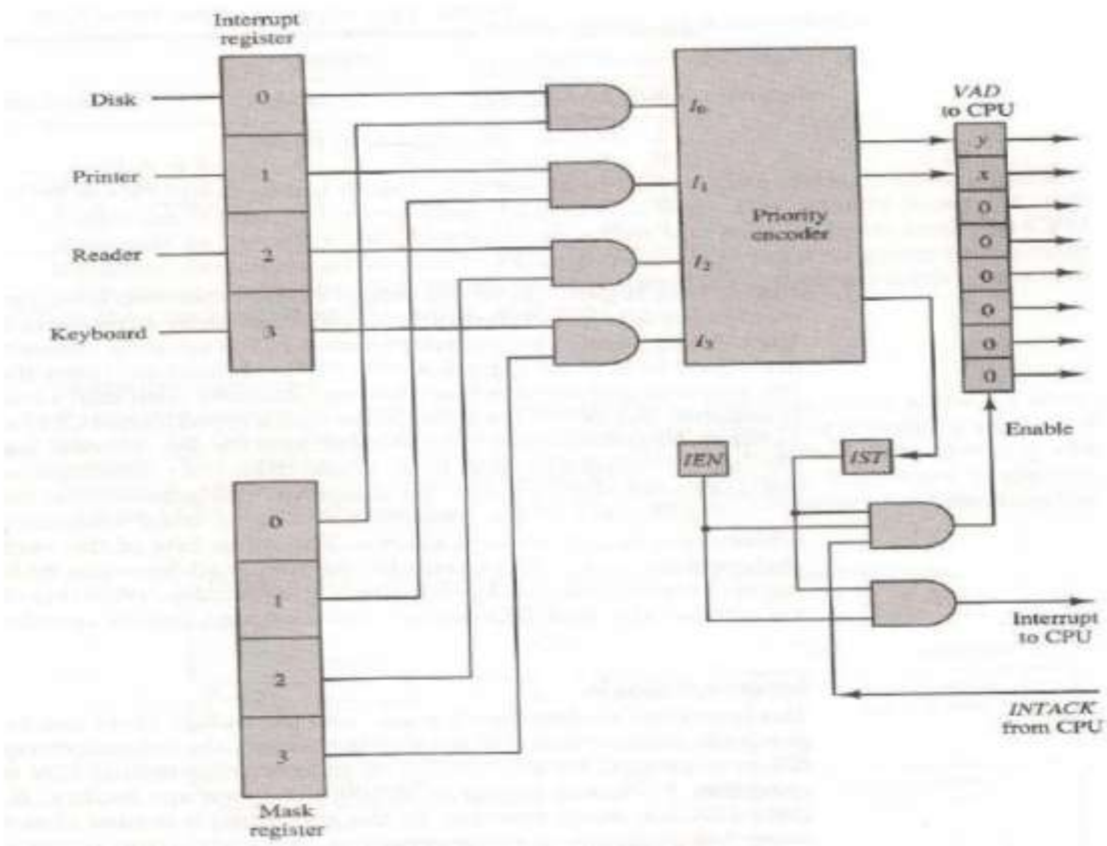

Fig: Priority Interrupt Hardware

It consists of:

- an interrupt register whose individual bits are set by external conditions and cleared by program instructions.
  - The magnetic disk, being a high-speed device is given the highest priority.
- the mask register has the same number of bits as the interrupt register. By means of program instructions, it is possible to set or reset any bit in the mask register.
- Each interrupt bit and it corresponding mask bit are applied to an AND gate to produce the four inputs to a priority encoder.

In this way an interrupt is recognized only if its corresponding mask bit is set to 1 by the program. The priority encoder generates two bits of the vector address, which is transferred to the CPU.

- Another output from the encoder sets an interrupt status flip-flop IST when an interrupt that is not masked occurs.
- The interrupt enable flip-flop IEN can be set or cleared by the program to provide an overall control over the interrupt system.
- The outputs of IST ANDed with IEN provide a common interrupt signal for the CPU.
- The interrupt acknowledge INTACK signal from the CPU enables the bus buffers in the output register and a vector address VAD is placed into the data bus.

The priority encoder is a circuit that implements the priority function. The logic of the priority encoder is such that if two or more inputs arrive at the same time, the input having the highest priority will take precedence.