Unit: 4
Input-Output Organization
Lecture-5
Direct Memory Access

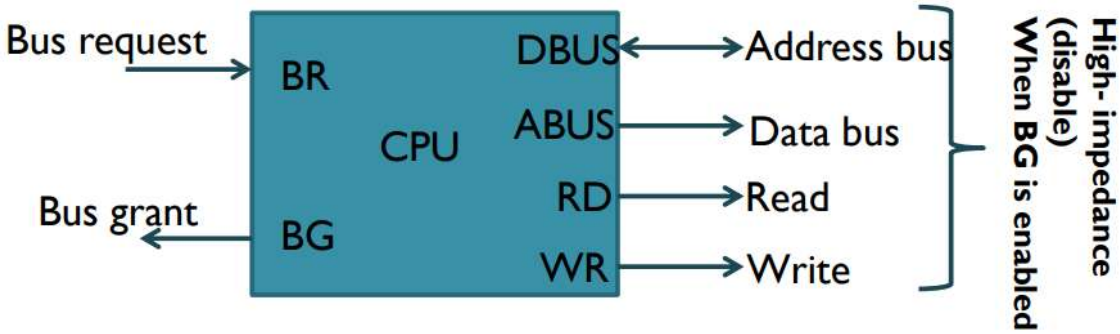
The transfer of data between a fast storage device such as magnetic disk and memory is often limited by the speed of the CPU. Removing the CPU from the path and letting the peripheral device manage the memory buses directly would improve the speed of transfer.

This transfer technique is called Direct Memory Access (DMA).

During the DMA transfer, the CPU is idle and has no control of the memory buses. A DMA Controller takes over the buses to manage the transfer directly between the I/O device and memory. The CPU may be placed in an idle state in a variety of ways.

One common method extensively used in microprocessor is to disable the buses through special control signals such as:

- Bus Request (BR)
- Bus Grant (BG)



These two control signals in CPU facilitates the DMA transfer.

- The Bus Request (BR) input is used by the DMA controller to request the CPU.
    - When this input is active, the CPU terminates the execution of the current instruction and places the address bus, data bus and read write lines into a high impedance state.
        - High impedance state means that the output is disconnected.
- The CPU activates the Bus Grant (BR) output to inform the external DMA that the Bus Request (BR) can now take control of the buses to conduct memory transfer without processor.

When the DMA terminates the transfer, it disables the Bus Request (BR) line. The CPU disables the Bus Grant(BG), takes control of the buses and return to its normal operation.

The transfer can be made in several ways:

- **DMA Burst:** In DMA Burst transfer, a block sequence consisting of a number of memory words is transferred in continuous burst while the DMA controller is master of the memory buses.
- **Cycle Stealing:** Cycle stealing allows the DMA controller to transfer one data word at a time, after which it must return control of the buses to the CPU. The CPU merely delays its operation for one memory cycle to allow the direct memory I/O transfer to steal one memory cycle.