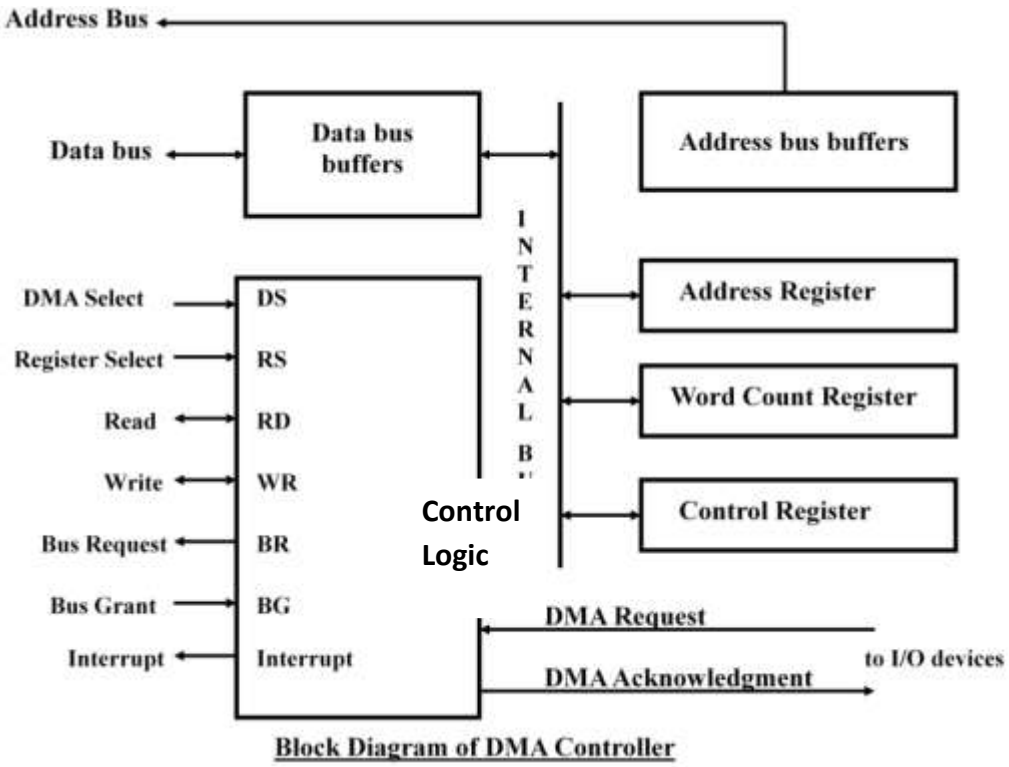
Unit: 4
Input-Output Organization
Lecture-6
DMA Controller and DMA Transfer

DMA Controller:

The DMA controller needs the usual circuits of an interface to communicate with the CPU and I/O device.



Block Diagram of DMA Controller

The DMA controller has three registers:

1. **Address Register:** contains an address to specify the desired location in memory.
2. **Word Count Register:** WC holds the number of words to be transferred. The register is decremented by one after each word transfer and internally tested for zero.
3. **Control Register:** specifies the mode of transfer

The unit communicates with the CPU via the data bus and control lines. The registers in the DMA are selected by the CPU through the address bus by enabling the DS (DMA select) and RS (Register select) inputs. The RD (read) and WR (write) inputs are bidirectional.

When the BG (Bus Grant) input is 0, the CPU can communicate with the DMA registers through the data bus to read from or write to the DMA registers. When BG =1, the DMA can communicate directly with the memory by specifying an address in the address bus and activating the RD or WR control.

DMA Transfer:

The position of DMA controller among the other components in a computer system is shown below:

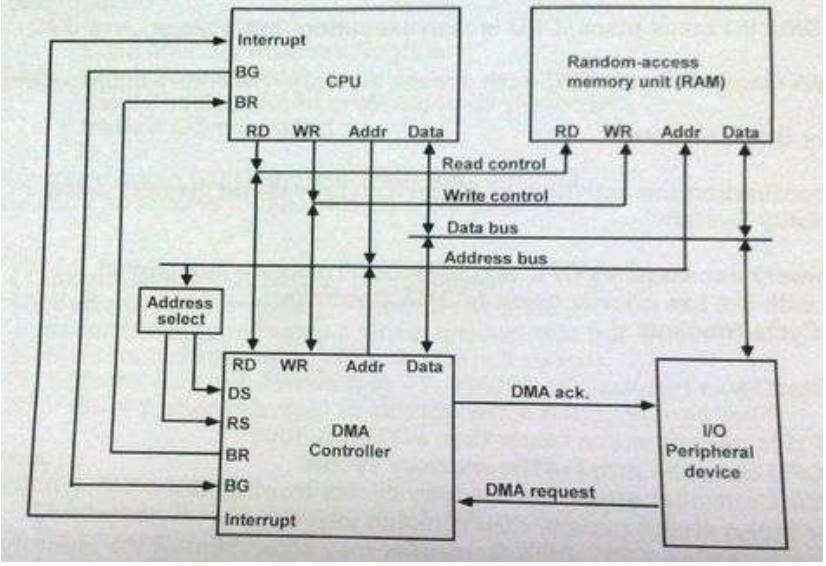


Fig: DMA transfer in computer system

The CPU communicates with the DMA through the address and data buses as with any interface unit. The DMA has its own address, which activates the DS and RS lines.
The CPU initializes the DMA through the data bus.
Once the DMA receives the start control command, it can start the transfer between the peripheral device and the memory.

- When the peripheral device sends a DMA request, the DMA controller activates the BR line, informing the CPU to relinquish the buses.
- The CPU responds with its BG line, informing the DMA that its buses are disabled.
- The DMA then puts the current value of its address register into the address bus, initiates the RD and WR signal, and sends a DMA acknowledge to the peripheral device.
    - RD and WR lines in the DMA controller are bidirectional
        - When BG = 0 → RD and WR are input lines allowing the CPU to communicate with the internal DMA registers.
        - When BG=1→ RD and WR are output lines form DMA controller to the random-access memory to specify the read or write operation for the data.
- When the peripheral device receives a DMA acknowledge, it puts a word in the data bus (for write) or receives a word from the data bus (for read).

Thus, the DMA controls the read or write operations and supplies the address for the memory. The peripheral unit can then communicate with memory through the data bus for direct transfer between the units while the CPU is momentarily disabled.