Lecture: 3

Timing and Control, Instruction Cycle

The timing for all registers in the basic computer is controlled by a master clock generator. The clock pulses are applied to all flip-flops and registers in the system, including the flip-flops and registers in the control unit. The clock pulses do not change the state of a register unless the register is enabled by a control signal.

The control signals are generated in the control unit and provide control inputs for the multiplexers in the common bus, control inputs in processor registers and micro-operations for the accumulator.

There are two major types of control organization:

- **Hardwired Control**
- **Micro-programmed Control**

Hardwired Control	Micro-programmed Control
The control logic is implemented with gates, flip-flops, decoders and other digital circuits.	The control information is stored in a control memory. The control memory is programmed to initiate the required sequence of micro operations.
The advantage is that it can be optimized to produce a fast mode of operation.	Compared with the hardwired control operation is slow.
Requires changes in the wiring among the various components if the design has to be modified or changed.	Required changes or modifications cn be done by updating the microprogram in control memory.

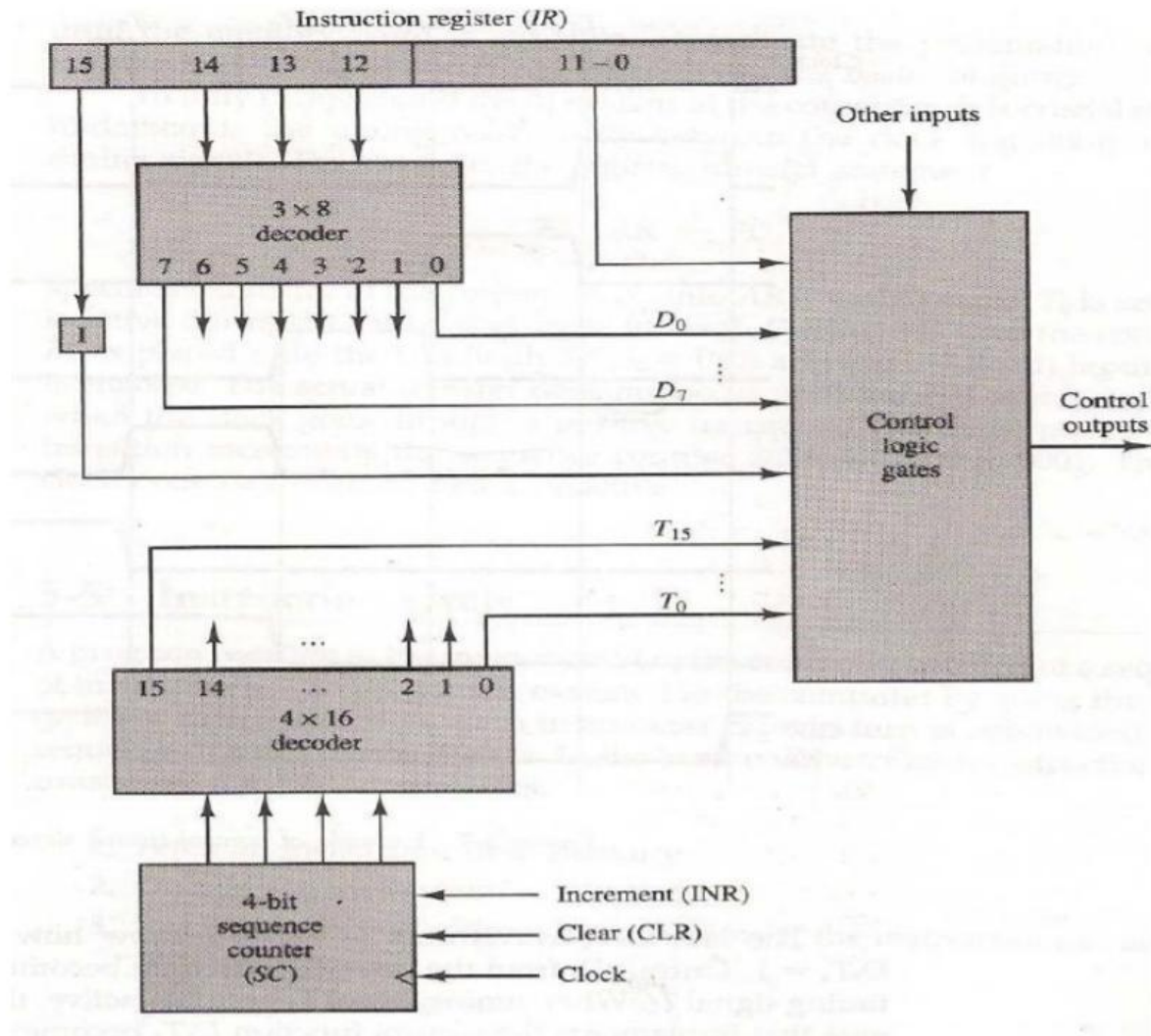The block diagram of the hardwired control unit is shown below:


Fig: Control Unit of Basic Computer

The control unit of basic computers consists of two decoders, a sequence counter and a number of control logic gates.

- An instruction read from memory is placed in the instruction register (IR). It is divided into three parts:
  - a. The I bit
  - b. The operation code and
  - c. Bits 0 through 11.
- The operation code in bits 12 through 14 are decoded with a 3*8 decoder. The eight outputs of the decoder are designated by the symbols D_0 through D_7.

- Bit 15 of the instruction is transferred to a flip-flop designated by the symbol I.
    - Bits 0 through 11 are applied to the control logic gates.
- The 4-bit sequence counter can count in binary from 0 through 15.
- The outputs of the counter are decoded into 16 timing signals T_0 through T_{15}.
- The sequence counter SC can be incremented or cleared synchronously.
- The counter is incremented to provide the sequence of timing signals out of the 4*16 decoder.

Instruction Cycle:

A program residing in the memory unit of the computer consists of a sequence of instructions. The program is executed in the computer by going through a cycle of each instruction. Each instruction cycle in turn is subdivided into a sequence of sub cycles or phases.
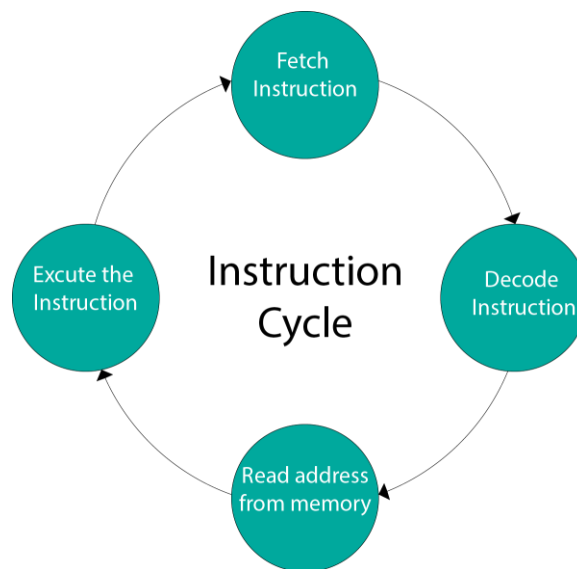
In the basic computer each instruction cycle consists of the following phases:

1. Fetch an instruction from memory.
2. Decode the instruction
3. Read the effective address from memory if the instruction has an indirect address.
4. Execute the instruction.

Upon the completion of step 4, the control goes back to step 1 to fetch, decode, and execute the next instruction.

1. **Fetch instruction**: Read instruction code from address in PC and place in IR. (IR ← Memory[PC])

2. **Decode instruction**: Hardware determines what the opcode/function is and determines which registers or memory addresses contain the operands.

3. **Fetch operands from the memory if necessary**: If any operands are memory addresses, initiate memory read cycles to read them into CPU registers. If an operand is in memory, not a register, then the memory address of the operand is known as the effective address (EA). The fetching of an operand can therefore be denoted as Register ← Memory[EA].

4. **Execute**: Perform the function of the instruction. If arithmetic or logic instruction, utilize the ALU circuits to carry out the operation on data in registers.