**Computer System Architecture**
**COMP201Th**
**Unit: 2**
**Basic Computer Organization and Design**

**Lecture: 4**

**General Register Organization**

Memory locations are needed for storing pointers, counters, return addresses, temporary results and partial products during operations. Having to refer to memory locations is time consuming because memory access is the most time-consuming operation in a computer.

It is more convenient and more efficient to store these intermediate values in processor registers.

When a large number of registers are included in the CPU, it is most efficient to connect them through a common bus system. The registers communicate with each other not only for direct data transfers, but also while performing various micro-operations.

A bus organization for seven CPU registers is as shown below:

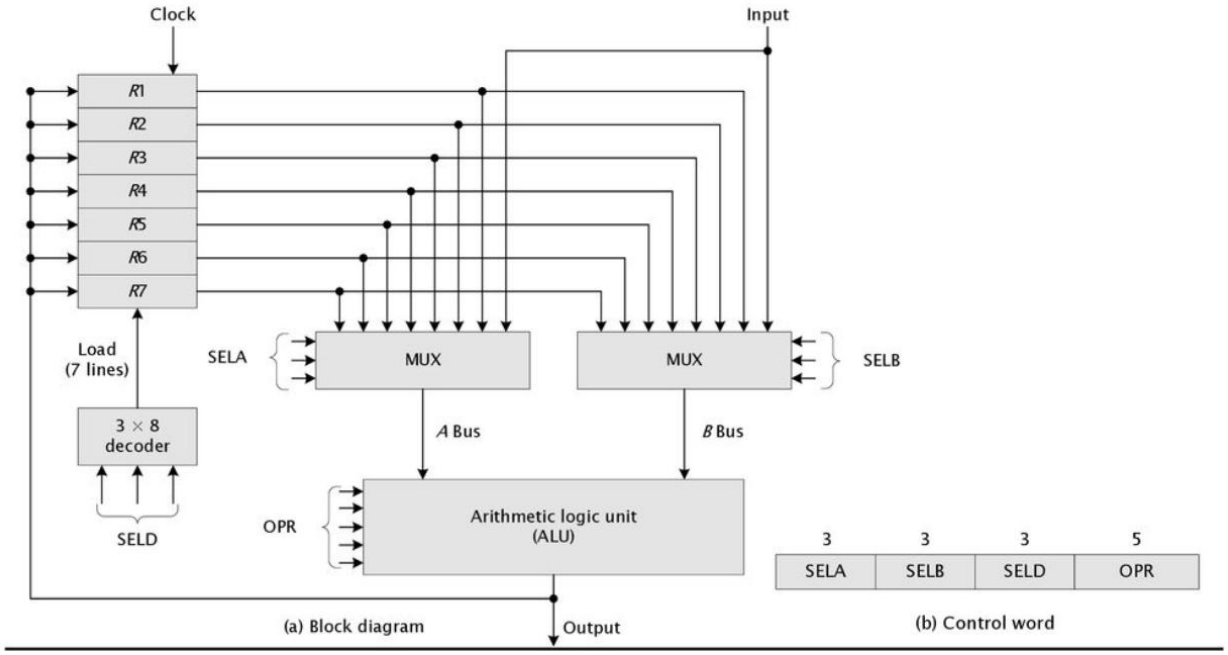


Fig: General Register Organization

The output of each register is connected to two multiplexers (MUX) to form the two buses A and B.

- The selection lines in each multiplexer select one register or the input data for the particular bus.

- The A and B buses form the inputs to a common arithmetic logic unit (ALU).
- The operation selected in the ALU determines the arithmetic or logic micro-operation that is to be performed.
- The result of the micro-operation is available for output data and also goes into the inputs of all the register.
- The register that received the information from the output bus is selected by a decoder. The decoder activates one of the register load inputs, thus providing a transfer path between the data in the output bus and the inputs of the selected destination register.

The control unit that operates the CPU bus system directs the information flow through the registers and ALU by selecting the various components in the system.

**Control Word:** There are 14 binary selection inputs in the unit, and their combined value specifies a control word.

It consists of four fields:

- The three bits of SELA select a source register for the A input of the ALU.
- The three bits of SELB select a register for the B input of the ALU.
- The three bits of SELD select a destination register using the decoder and its seven load outputs.
- The five bits of OPR select one of the operations in ALU.

The 14-bit control word when applied to the selection inputs specify a particular micro-operation.

**Encoding of Register Selection Fields:**

| Binary Code | SELA | SELB | SELD |
|---|---|---|---|
| 000 | Input | Input | None |
| 001 | R1 | R1 | R1 |
| 010 | R2 | R2 | R2 |
| 011 | R3 | R3 | R3 |
| 100 | R4 | R4 | R4 |
| 101 | R5 | R5 | R5 |
| 110 | R6 | R6 | R6 |
| 111 | R7 | R7 | R7 |

Table: Encoding of Register Selection Fields

The 3-bit binary code listed in the first column of the table specifies the binary code for each of the three fields. The register selected by fields SELA, SELB and SELD is the one whose decimal number is equivalent to the binary number in the code.

When SELA or SELB is 000, the corresponding multiplexer selects the external input data.

When SELD=000, no destination register is selected but the contents of the output bus are available in the external output.

**Encoding of ALU Operations:**

| OPR Select | Operation | Symbol |
|---|---|---|
| 00000 | Transfer *A* | TSFA |
| 00001 | Increment *A* | INCA |
| 00010 | Add *A* + *B* | ADD |
| 00101 | Subtract *A* − *B* | SUB |
| 00110 | Decrement *A* | DECA |
| 01000 | AND *A* and *B* | AND |
| 01010 | OR *A* and *B* | OR |
| 01100 | XOR *A* and *B* | XOR |
| 01110 | Complement *A* | COMA |
| 10000 | Shift right *A* | SHRA |
| 11000 | Shift left *A* | SHLA |

Table: Encoding of ALU Operations

The ALU provides arithmetic and logic operations. The function table for this ALU is shown in above table. The OPR field has five bits and each operation is designated with a symbolic name.

**Example:** To perform the operation: R1 ← R2+R3

The control must provide binary selection variables to the following selector inputs:

1. MUX A selector (SELA): to place the content of R2 into bus A.
2. MUX B selector (SELB): to place the content of R3 into bus B.
3. ALU operation selector (OPR): to provide the arithmetic addition A+B.
4. Decoder destination selector (SELD): to transfer the content of the output bus into R1.

A control word of 14 bits is needed to specify this micro-operation.

| Field: | SELA | SELB | SELD | OPR |
|---|---|---|---|---|
| Symbol: | R2 | R3 | R1 | ADD |
| Control Word | 010 | 011 | 001 | 00010 |