# Computer System Architecture <br> COMP201Th <br> Unit: 2 <br> Basic Computer Organization and Design <br> Lecture: 5 <br> <br> Arithmetic Micro-operations 

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The basic set of arithmetic micro-operations are:

| Symbolic <br> designation | Description |
| :--- | :--- |
| $R 3 \leftarrow R 1+R 2$ | Contents of $R 1$ plus $R 2$ transferred to $R 3$ |
| $R 3 \leftarrow R 1-R 2$ | Contents of $R 1$ minus $R 2$ transferred to $R 3$ |
| $R 2 \leftarrow \overline{R 2}$ | Complement the contents of $R 2$ (l's complement) |
| $R 2 \leftarrow \overline{R 2}+1$ | 2's complement the contents of $R 2$ (negate) |
| $R 3 \leftarrow R 1+\overline{R 2}+1$ | $R 1$ plus the 2's complement of $R 2$ (subtraction) |
| $R 1 \leftarrow R 1+1$ | Increment the contents of $R 1$ by one |
| $R 1 \leftarrow R 1-1$ | Decrement the contents of $R 1$ by one |

Note: The arithmetic operations of multiply and divide are not listed in above table. These two operations are valid arithmetic operations but are not included in the basic set of micro-operations. In most computers, the multiplication operation is implemented with a sequence of add and shift micro-operations. Division is implemented with a sequence of subtract and shift micro-operations.

The arithmetic micro-operations listed in above table can be implemented in one composite arithmetic circuit.

The basic component of an arithmetic circuit is the parallel adder. By controlling the data inputs to the adder, it is possible to obtain different types of arithmetic operations.

The diagram of a 4-bit arithmetic circuit is shown below:


Fig: 4-bit arithmetic circuit

- It has four full-adder circuits that constitute the 4-bit adder and four multiplexers for choosing different operations.
- There are two 4-bit inputs A and B and a 4-bit output D.
- The four inputs from A go directly to the X inputs of the binary adder.
- Each of the four inputs from B are connected to the data inputs of the multiplexers. The multiplexers data inputs also receive the complement of B.
- The other two data inputs are connected to logic-0 and logic-1.
- Logic-0 is a fixed voltage value and the logic- 1 signal can be generated through an inverter whose input is 0 .
- The four multiplexers are controlled by two selection inputs, $\mathrm{S}_{1}$ and $\mathrm{S}_{0}$.
- The input carry $\mathrm{C}_{\mathrm{in}}$ goes to the carry input of the FA in the least significant position. The other carries are connected from one stage to the next.

The output of the binary adder is calculated from the following arithmetic sum:

$$
\mathbf{D}=\mathbf{A}+\mathbf{Y}+\mathbf{C}_{\mathrm{in}}
$$

Where,

- A is the 4 bit binary number at the $X$ inputs and
- Y is the 4-bit binary number at the $Y$ inputs of the binary adder
- And $\mathrm{C}_{\mathrm{in}}$ is the input carry, which can be equal to 0 or 1 .

By controlling the value of Y with the two selection inputs S1 and S0 and making $C_{\text {in }}$ equal to 0 or 1 , it is possible to generate the eight arithmetic microoperations as shown below:

| Select |  |  |  |  |  |
| :--- | :---: | :---: | :---: | :--- | :--- |
| $S_{1}$ | $S_{0}$ | $C_{\text {in }}$ | Input | $Y$ | Output |
| 0 | 0 | 0 | $B$ | $D=A+B$ | Microoperation |
| 0 | 0 | 1 | $B$ | $D=A+B+1$ | Add with carry |
| 0 | 1 | 0 | $\bar{B}$ | $D=A+\bar{B}$ | Subtract with borrow |
| 0 | 1 | 1 | $\bar{B}$ | $D=A+\bar{B}+1$ | Subtract |
| 1 | 0 | 0 | 0 | $D=A$ | Transfer $A$ |
| 1 | 0 | 1 | 0 | $D=A+1$ | Increment $A$ |
| 1 | 1 | 0 | 1 | $D=A-1$ | Decrement $A$ |
| 1 | 1 | 1 | 1 | $D=A$ | Transfer $A$ |

Arithmetic Circuit Function Table

